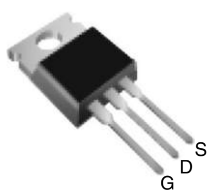
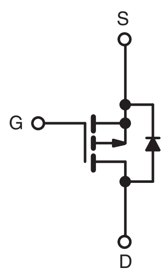
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	3.0
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	4.0	
Configuration	Single	

TO-220





P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRF9610PbF
	SiHF9610-E3
SnPb	IRF9610
	SiHF9610

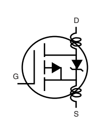
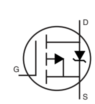
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25	I_D	- 1.8	A
		T_C = 100		- 1.0	
Pulsed Drain Current[a]			I_{DM}	- 7.0	
Linear Derating Factor				0.16	W/°C
Maximum Power Dissipation	T_C = 25 °C		P_D	20	W
Inductive Current, Clamp			I_{LM}	- 7.0	A
Peak Diode Recovery dV/dt[c]			dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).
b. Not applicable.
c. $I_{SD} \leq$ - 1.8 A, dI/dt ≤ 70 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	6.4	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA	-	- 0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 200 V, V_{GS} = 0 V	-	-	- 100	µA
		V_{DS} = - 160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V; I_D = -0.90 A[b]	-	-	3.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 50 V, I_D = - 0.90 A[b]	0.90	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 10	-	170	-	pF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V; I_D = - 3.5 A, V_{DS} = - 160 V, see fig. 11 and 18[b]	-	-	11	nC
Gate-Source Charge	Q_{gs}		-	-	7.0	
Gate-Drain Charge	Q_{gd}		-	-	4.0	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 100 V, I_D = - 0.90 A, R_G = 50 Ω, R_D = 110 Ω, see fig. 17[b]	-	8.0	-	ns
Rise Time	t_r		-	15	-	
Turn-Off Delay Time	$t_{d(off)}$		-	10	-	
Fall Time	t_f		-	8.0	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 1.8	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	- 7.0	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 1.8 A, V_{GS} = 0 V[b]	-	-	- 5.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 1.8 A, dI/dt = 100 A/µs[b]	-	240	360	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.7	2.6	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

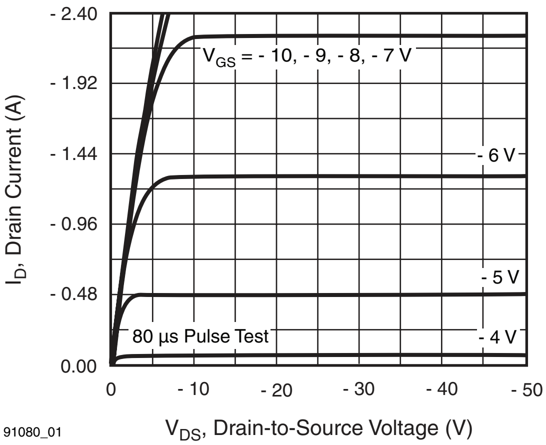


Fig. 1 - Typical Output Characteristics

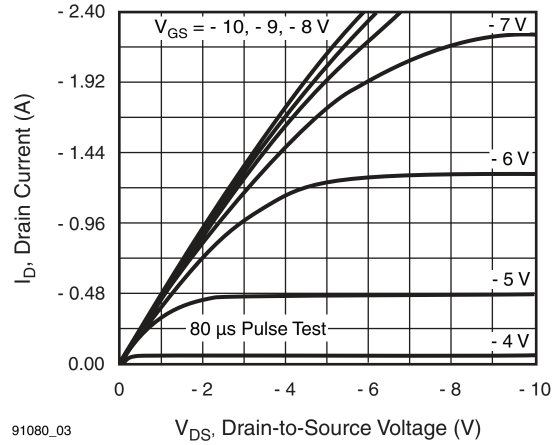


Fig. 3 - Typical Saturation Characteristics

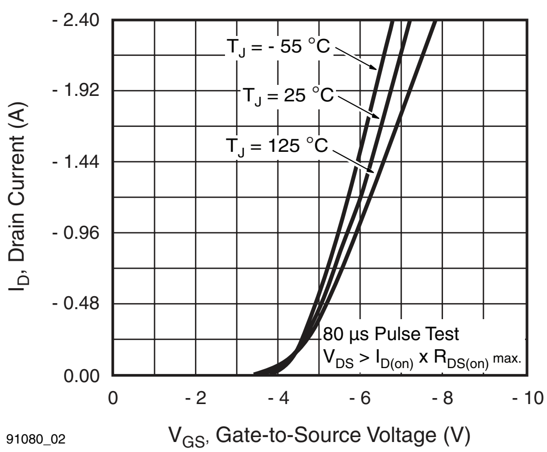


Fig. 2 - Typical Transfer Characteristics

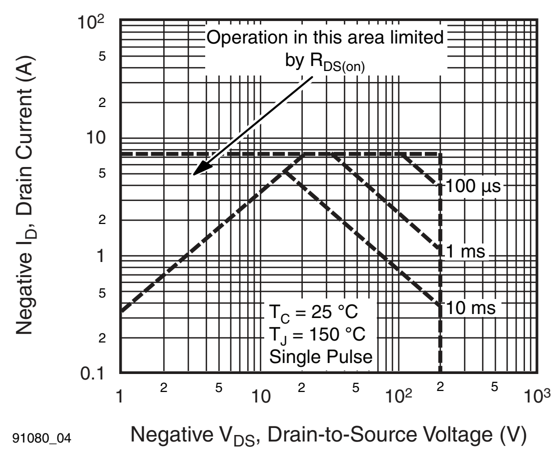


Fig. 4 - Maximum Safe Operating Area

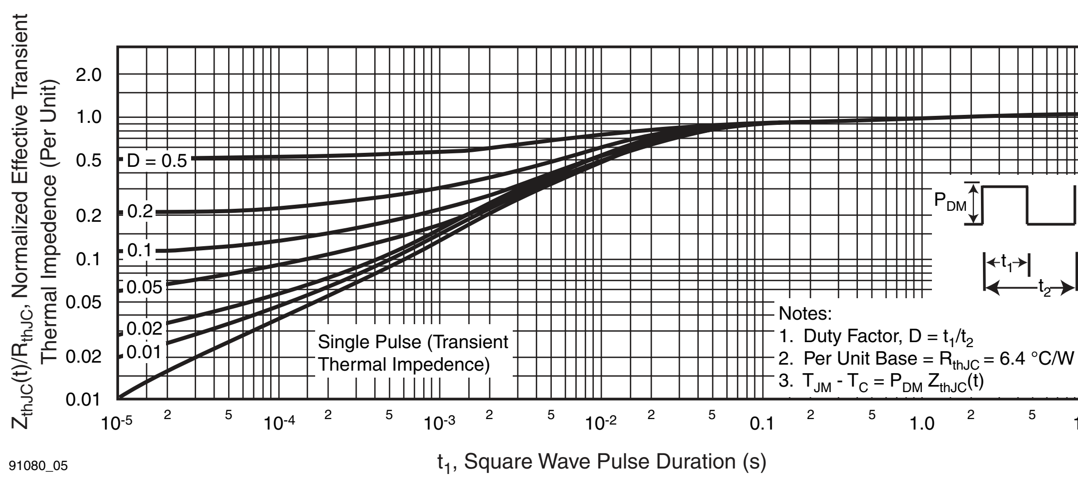


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

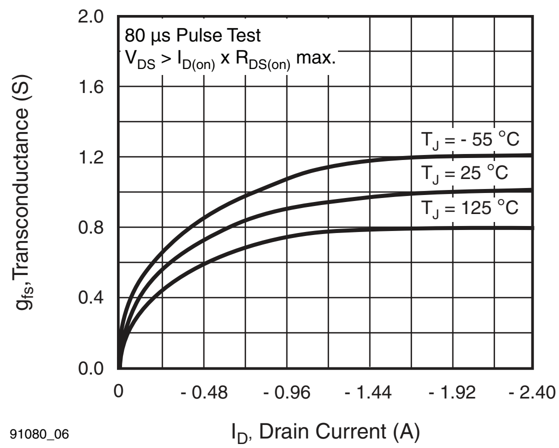


Fig. 6 - Typical Transconductance vs. Drain Current

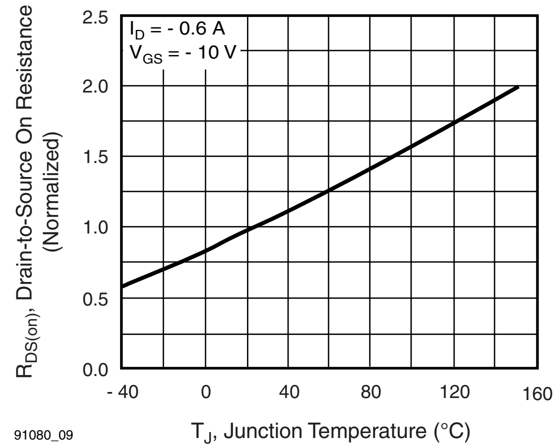


Fig. 9 - Normalized On-Resistance vs. Temperature

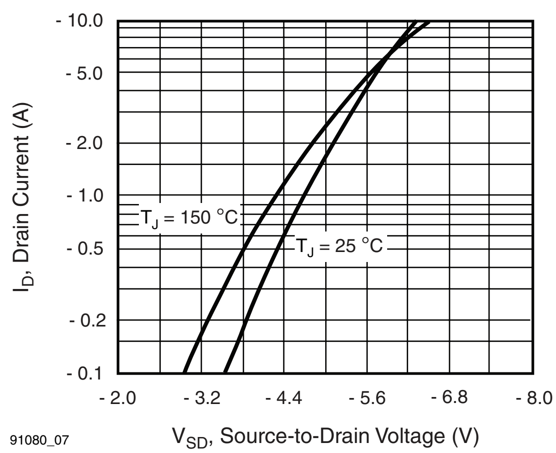


Fig. 7 - Typical Source-Drain Diode Forward Voltage

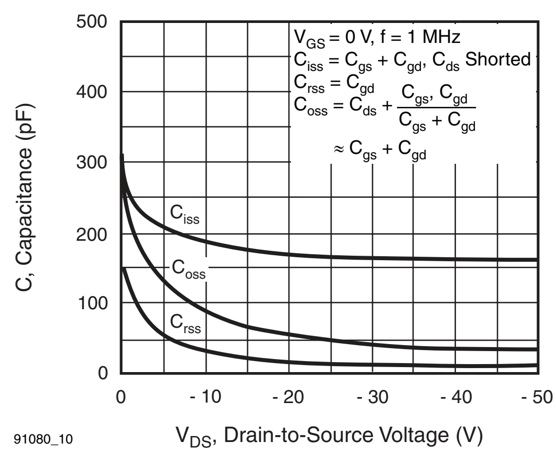


Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

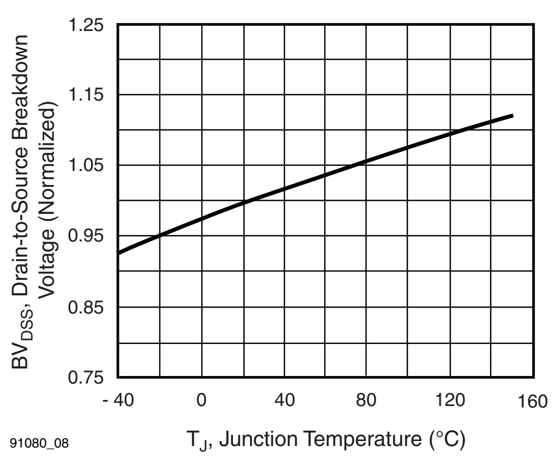


Fig. 8 - Breakdown Voltage vs. Temperature

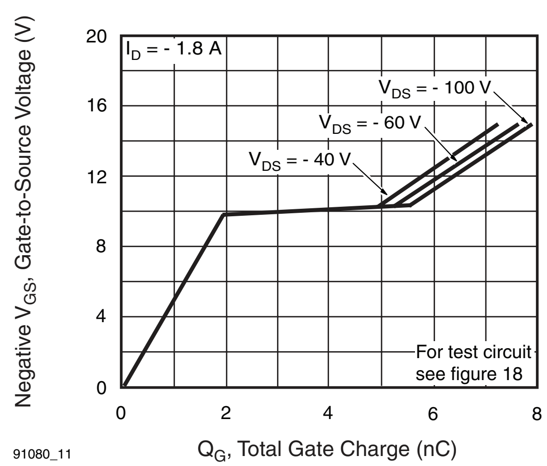


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

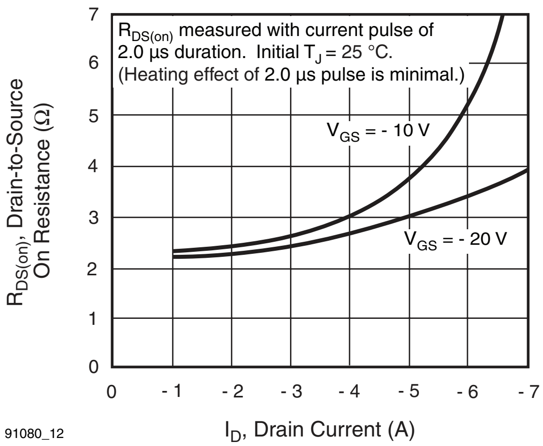


Fig. 12 - Typical On-Resistance vs. Drain Current

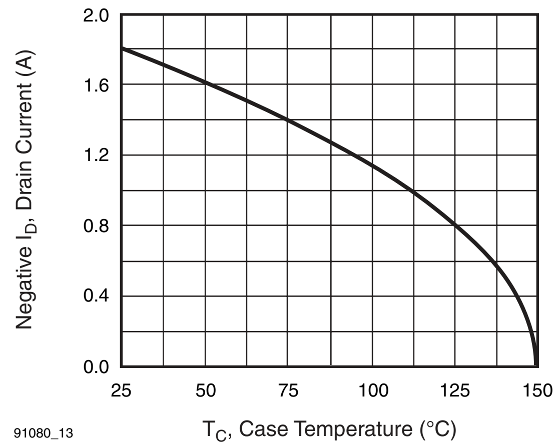


Fig. 13 - Maximum Drain Current vs. Case Temperature

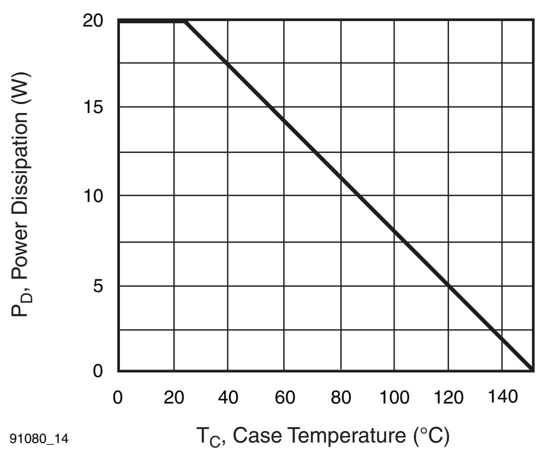


Fig. 14 - Power vs. Temperature Derating Curve

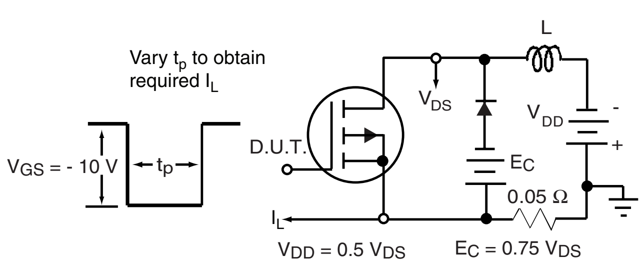


Fig. 15 - Clamped Inductive Test Circuit

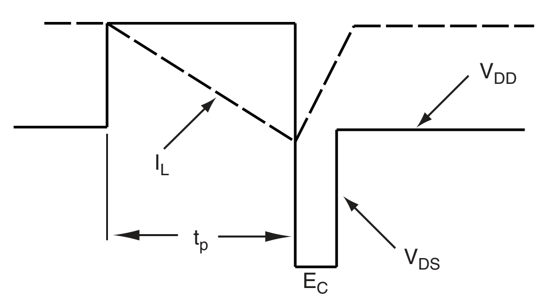


Fig. 16 - Clamped Inductive Waveforms

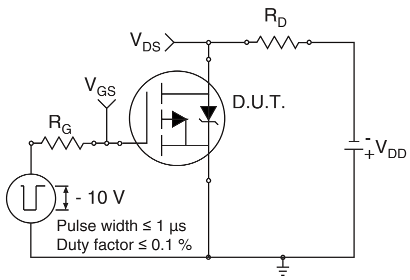


Fig. 17a - Switching Time Test Circuit

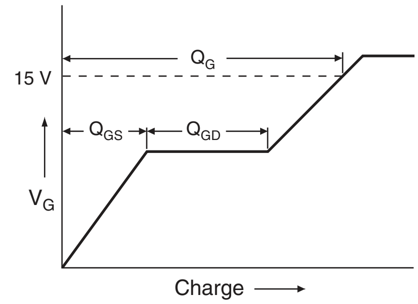


Fig. 18a - Basic Gate Charge Waveform

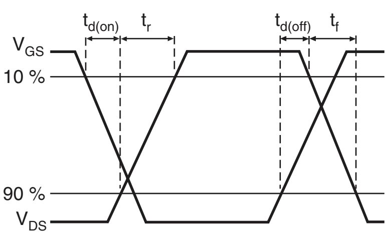


Fig. 17b - Switching Time Waveforms

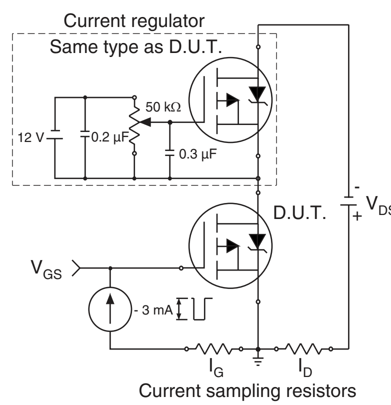
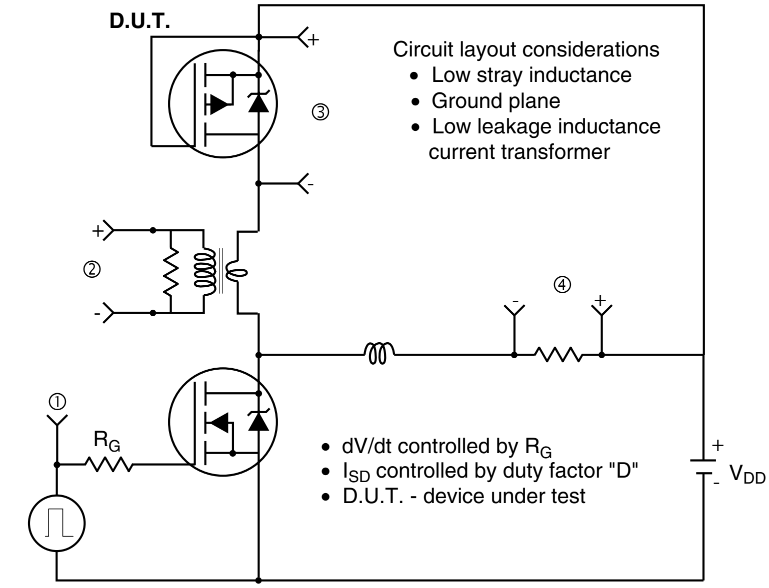
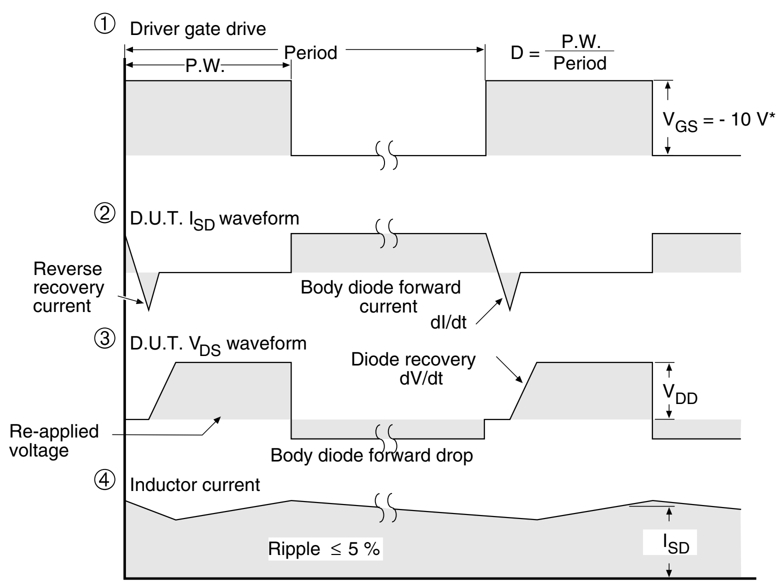


Fig. 18b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver

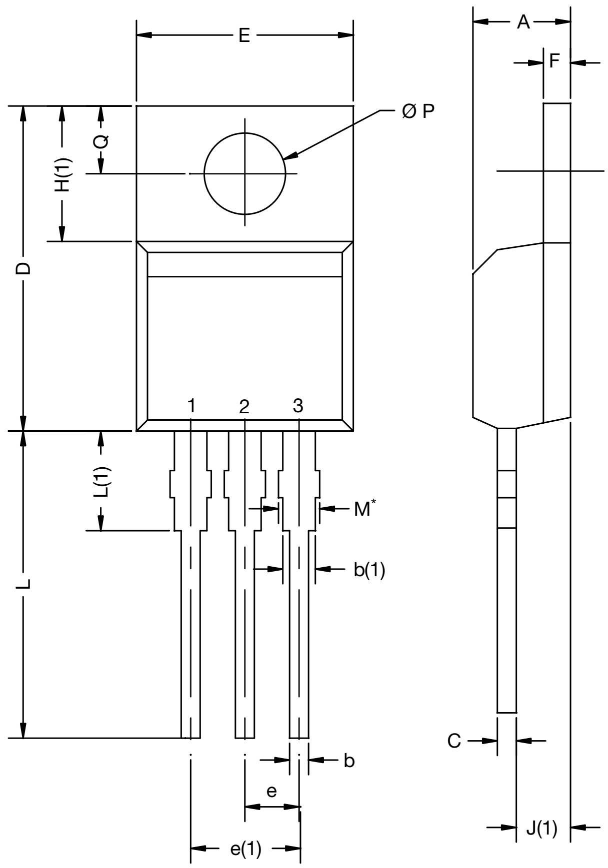


* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 19 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91080.

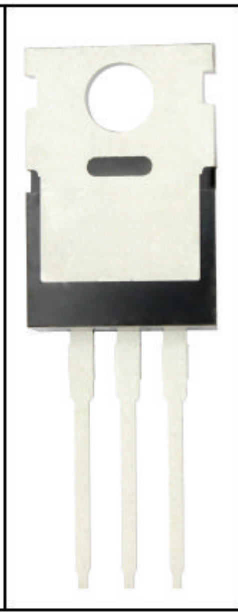
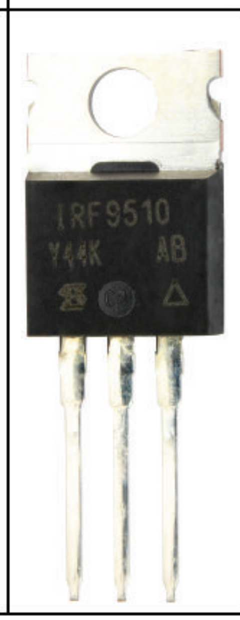
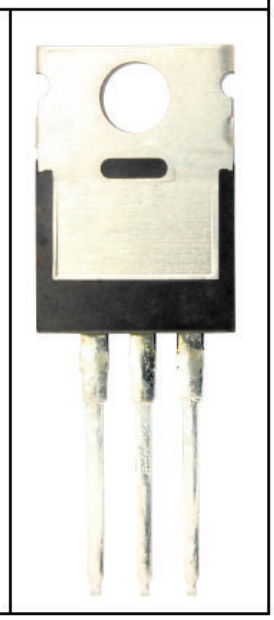
TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture			
ASE		Xi'an	
			

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